

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	("KURAKANE,HIROSHI").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2007/02/16 14:17
S2	20	"KURAKANE, HIROSHI"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:19
S3	27118	"NEC CORPORATION"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:20
S4	1	S3 and (("clock" adj "control" adj ("system" or "device" or "unit" or "apparatus" or "method")) with ("frequency" adj ("multiplication" or "division") adj circuit\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:41
S5	0	S3 and (("clock" adj "control" adj ("system" or "device" or "unit" or "apparatus" or "method")) with ("frequency" adj circuit\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:24
S6	2	((("clock" adj "control" adj ("system" or "device" or "unit" or "apparatus" or "method")) with ("frequency" adj ("multiplication" or "division") adj circuit\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:25
S7	2	"6742133"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:34
S8	3	"7000140"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:36
S9	11	"5524035"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:36
S10	1500	713/322	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:41

EAST Search History

S11	0	S10 and (("clock" adj "control" adj ("system" or "device" or "unit" or "apparatus" or "circuit" or "method"))) with ("frequency" adj ("multiplication" or "division") adj circuit\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:50
S12	1	S10 and (("clock" with "control" adj ("system" or "device" or "unit" or "apparatus" or "circuit" or "method"))) with ("frequency" adj ("multiplication" or "division") adj circuit\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:51
S13	1	S10 and (("clock" with "control" with ("system" or "device" or "unit" or "apparatus" or "circuit" or "method"))) with ("frequency" adj ("multiplication" or "division") adj circuit\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:53
S14	179	S10 and (("clock" with control\$3) with ("frequency" with circuit\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:55
S15	4	S14 and ("frequency" adj ("multiplication" or "division") adj circuit\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:55
S16	2363	713/320	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:54
S17	120	S16 and (("clock" with control\$3) with ("frequency" with circuit\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:56
S18	4	S17 and ("frequency" adj ("multiplication" or "division") adj circuit\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:56
S19	180	327/39	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:56
S20	28	S19 and (("clock" with control\$3) with ("frequency" with circuit\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:57
S21	2	S20 and ("frequency" adj ("multiplication" or "division") adj circuit\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:57

EAST Search History

S22	672	327/115	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:57
S23	133	S22 and (("clock" with control\$3) with ("frequency" with circuit\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:58
S24	6	S23 and ("frequency" adj ("multiplication" or "division") adj circuit\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:58
S25	620	327/116	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:58
S26	131	S25 and (("clock" with control\$3) with ("frequency" with circuit\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:59
S27	2	S26 and ("frequency" adj ("multiplication" or "division") adj circuit\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:59
S28	383	327/114	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:59
S29	73	S28 and (("clock" with control\$3) with ("frequency" with circuit\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:59
S30	5	S29 and ("frequency" adj ("multiplication" or "division") adj circuit\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 15:00
S31	891	327/142	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 14:59
S32	57	S31 and (("clock" with control\$3) with ("frequency" with circuit\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 15:00
S33	2	S32 and ("frequency" adj ("multiplication" or "division") adj circuit\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/02/16 15:00

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clock control system with frequency multiplicat

Search Patents

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[Google Patent Searc](#)"with" is a very common word and was not included in your search. [\[details\]](#)**Patent Search** Patents 1 - 10 of 614 on **clock control system with frequency multiplication division cir****Data processor and data processing system**

US Pat. 7000140 - Filed Nov 27, 2001 - Renesas Technology Corporation

In the standby mode, the **frequency multiplication** and **frequency division** ...When the **control** signal 33 is at the high level, the **clock output circuits** 47, ...**Symmetric clock system for a data processing system including dynamically switchable frequency divider**

US Pat. 5524035 - Filed Aug 10, 1995 - International Business Machines Corporation

1 is a block diagram of the **clock control** circuit in accordance with the present invention including off/even **frequency division** with symmetric output. FIG. ...**Efficient communication system using time division multiplexing and timing adjustment control**

US Pat. 6366566 - Filed Jul 8, 1999 - Xircom Wireless, Inc.

The master oscillator **frequency** is designated in FIG. 19B as fo. M and M2 are programmable divide ratios for **clock divider circuits** 1926 and 1927. ...**Efficient communication system using time division multiplexing and timing adjustment control**

US Pat. 6049538 - Filed Jun 16, 1997 - Omnipoint Corporation

The master oscillator **frequency** is designated in FIG. 19B as fo. M and M2 are programmable divide ratios for **clock divider circuits** 1926 and 1927. ...**Efficient frequency division duplex communication system with interleaved format and timing adjustment control**

US Pat. 5689502 - Filed Jun 5, 1995 - Omnipoint Corporation

The **frequency** multiplier M2 are programmable divide ratios for **clock divider** ...IF signal 45 In an alternative embodiment, one or more **system control** 1946. ...**Efficient communication system using time division multiplexing and timing adjustment control**

US Pat. 5745484 - Filed Jun 5, 1995 - Omnipoint Corporation

The **frequency** multiplier M2 are programmable divide ratios for **clock divider circuits** circuit 1935 is connected to a multiplier 1936, which mul- 50 1926 and ...**Clock controlling method and clock control circuit**

US Pat. 6742133 - Filed Nov 14, 2001 - NEC Electronics Corporation

As a **clock control** circuit, a feedback type circuit, such as FIG- 13 shows> as... includes a **frequency** divider 2 for dividing **division circuits** 208 to 215, ...**Efficient time division duplex communication system with interleaved format and timing adjustment control**

US Pat. 5802046 - Filed Jun 5, 1995 - Omnipoint Corporation

The A/D In an alternative embodiment, one or more **system control** converter ...
for **clock divider circuits** between polling messages from the base station 304 ...

Clock controlling method and circuit with a multi-phase multiplication clock generating circuit

US Pat. 6791386 - Filed Feb 20, 2003 - NEC Electronics Corporation

A **clock control** circuit comprising: a multi-phase **multiplication clock** ...
ing: a plurality of timing difference **division circuits** for outputting a signal ...

Clock generation system

US Pat. 7084712 - Filed Aug 17, 2004 - Rohm Co., Ltd.

The first **frequency division** factor **control** circuit may have a first flip-flop
... 1, there is shown a **clock generation system** utilizing PLL **circuits** in ...

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Result Page: 1 2 3 4 5 6 7 8 9 10 **Next**

clock control system with frequency multiplica

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